

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: David E. Lackey

Art Unit:

Serial No.:

Dkt. No.: BUR920000170US2

Filed:

Examiner:

Title: **METHOD FOR INSERTION OF TEST POINTS INTO INTEGRATED LOGIC
CIRCUIT DESIGNS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Preliminary Amendment

Sir:

Kindly enter this amendment prior to initial examination

In the Specification:

The title is amended as follows:

METHOD FOR INSERTION OF TEST POINTS INTO INTEGRATED ~~CIRCUIT~~
LOGIC CIRCUIT DESIGNS

Page 1, between lines 1 and 2, insert: --This application is a divisional of Serial No.
09/788,925; filed on 2/20/2001.--

Please replace the fourth and fifth paragraphs on Page 9 of the specification with the
following paragraphs:

FIG. 9 is a flowchart illustrating the method steps for inserting test points into a logic
circuit design according to the present invention; and

FIG. 10 is a flowchart illustrating the method steps of an alternative methodology for inserting test points into a logic circuit design according to the present invention.